IN THE NOTICE OF ALLOWANCE

Please amend Claim 23 as indicated below:

Claim 23 (currently amended) A system, comprising:

(a) a shared memory; and

(b) two or more processing elements coupled to said shared memory, wherein two or more of said processing elements comprise:

(1) a processing unit, wherein said ~~central~~ processing unit comprises a first address translation mechanism[[,]];

(2) a direct memory access controller coupled to said processing unit, wherein said direct memory access controller comprises a second address translation mechanism; and

(3) at least one attached processing unit coupled to said direct memory access [[memory]] controller, wherein said at least one attached processing unit does not comprise an address translation mechanism.